In the Claims:

1. (Currently Amended) A semiconductor device comprising:

an insulator layer;

a planar transistor formed on a first portion of a semiconductor layer, the first portion of the semiconductor layer overlying the insulator layer, and the first portion of the semiconductor layer having a first thickness; and

a multiple-gate transistor formed on a second portion of the semiconductor layer, the second portion of the semiconductor layer overlying the insulator layer, the second portion of the semiconductor layer having a second thickness, and the second thickness being larger than the first thickness, wherein the multiple-gate transistor comprises:

a vertical semiconductor fin formed from the second portion of the semiconductor layer;

a gate dielectric having vertical portions on opposite sidewalls of a channel portion of the semiconductor fin and a horizontal portion on a top surface of the channel portion of the semiconductor fin;

a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric; and

source and drain regions formed in the second portion of the semiconductor layer oppositely adjacent the gate electrode.

2. (Original) The semiconductor device of claim 1, wherein the semiconductor layer comprises a material selected from a group consisting of silicon, germanium, silicon germanium, and combinations thereof.

3. (Original) The semiconductor device of claim 1, wherein the insulator layer comprises silicon oxide.

4. (Original) The semiconductor device of claim 1, wherein the first thickness is less than about 400 angstroms.

5. (Original) The semiconductor device of claim 1, wherein the second thickness is greater than about 100 angstroms.

6. (Original) The semiconductor device of claim 1, wherein the planar transistor comprises:

a planar channel formed from the first portion of the semiconductor layer;

a gate dielectric overlying at least a portion of the planar channel;

a gate electrode overlying the gate dielectric; and

source and drain regions formed in the first portion of the semiconductor layer oppositely adjacent the gate electrode.

7. (Currently Amended) The semiconductor device of claim 6, wherein the gate dielectric of the planar transistor comprises a material selected from a group consisting of

silicon oxide, silicon oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.

8. (Currently Amended) The semiconductor device of claim 6, wherein the gate electrode of the planar transistor comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.

9. (Cancelled)

10. (Currently Amended) The semiconductor device of claim [[9]] 1, wherein the gate dielectric of the multiple-gate transistor comprises a material selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.

11. (Currently Amended) The semiconductor device of claim [[9]] 1, wherein the gate electrode of the multiple-gate transistor comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.

12. (Original) The semiconductor device of claim 1, wherein corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors.

13. (Currently Amended) A semiconductor device comprising:

an insulator layer;

a first portion of a semiconductor layer having a first thickness, the first portion of the semiconductor layer overlying the insulator layer;

a second portion of the semiconductor layer having a second thickness, the second portion of the semiconductor layer overlying the insulator layer, and the second thickness being larger than the first thickness;

a first transistor having a first active region formed from the first portion of the semiconductor layer; and

a second transistor having a second active region formed from the second portion of the semiconductor layer, wherein the first transistor is a planar transistor, and the second transistor is a tri-gate transistor comprising a horizontal gate formed at a top surface of the second portion of the semiconductor layer, and two vertical gates formed at sidewalls of the second portion of the semiconductor layer.

14. (Currently Amended) The semiconductor device of claim 13, wherein the first thickness is less than about 400 angstroms, and the second thickness is [[of]] greater than about 100 angstroms.

15. (Cancelled)

16. (Original) The semiconductor device of claim 13, wherein corners of the first and second active regions are rounded.

17. (Currently Amended) A semiconductor device comprising:

an insulator layer;

a first portion of the semiconductor layer having a first thickness of less than about 400 angstroms, the first portion of the semiconductor layer overlying the insulator layer;

a second portion of the semiconductor layer having a second thickness of greater than about 100 angstroms, the second portion of the semiconductor layer overlying the insulator layer, and the second thickness being larger than the first thickness;

a first transistor having a first active region formed from the first portion of the semiconductor layer; and

a second transistor having a second active region formed from the second portion of the semiconductor layer, wherein the first transistor is a planar transistor, and the second transistor is a multiple-gate transistor comprising:

a vertical semiconductor fin formed from the second portion of the semiconductor layer;

a gate dielectric having vertical portions on opposite sidewalls of a channel portion of the semiconductor fin and a horizontal portion on a top surface of the channel portion of the semiconductor fin;

a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion

on the horizontal portion of the gate dielectric; and

source and drain regions formed in the second portion of the semiconductor layer oppositely adjacent the gate electrode.

18-37. (Cancelled)

38. (New) The semiconductor device of claim 6, wherein the gate dielectric of the planar transistor comprises a portion on a top surface of the planar channel and portions on sidewalls of the planar channel.

39. (New) A semiconductor device comprising:

an insulator layer;

a planar transistor formed on a first portion of a semiconductor layer, the first portion of the semiconductor layer overlying the insulator layer, and the first portion of the semiconductor layer having a first thickness;

a multiple-gate transistor formed on a second portion of the semiconductor layer, the second portion of the semiconductor layer overlying the insulator layer, the second portion of the semiconductor layer having a second thickness, and the second thickness being larger than the first thickness; and

the planar transistor comprising:

a planar channel formed from the first portion of the semiconductor layer;

a gate dielectric having vertical portions on opposite sidewalls of the planar channel and a horizontal portion on a top surface of the planar channel;

a gate electrode overlying the gate dielectric, wherein the gate electrode has vertical portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric; and

source and drain regions formed in the second portion of the semiconductor layer oppositely adjacent the gate electrode.